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#16 Appeal Brief

TRANSMITTAL OF APPEAL BRIEF (Large Entity)	Docket No. 901.0013.USU

In Re Application Of: **Cannata et al.**

Serial No.	Filing Date	Examiner	Group Art Unit
09/667,826	September 21, 2000	Hannaher, C.	2878

Invention:

Infrared Imaging System Employing On-Focal Plane Nonuniformity Correction

COPY OF PAPERS ORIGINALLY FILED

6/19/02

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on

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Signature

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I certify that this document and fee is being deposited on **June 10, 200** with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPLICANT: Cannata et al.

SERIAL NO.: 09/667,826 ART UNIT: 2878

FILED: 9/21/00 EXAMINER: Hannaher, C.

TITLE: Infrared Imaging System Employing On-Focal Plane Non-uniformity Correction

ATTORNEY DOCKET NO.: 901.0013 USU

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Brief For Appellants

Sir:

This is an appeal brief in regard to the final rejection of the claims in the above-identified patent application. A Notice of Appeal was mailed to the USPTO on April 11, 2002. The brief is being filed in triplicate as required by 37 C.F.R. 1.192. The fee described in 37 C.F.R. 1.17(c) is enclosed. Please charge deposit account 50-1924 for any fee deficiency.

I. Real Party In Interest

The real party in interest is Raytheon Systems Company.

II. Related Appeals and Interferences

There are no directly related appeals or interferences regarding this application.

III. Status of Claims

Claims 1-35, and 40-58 are pending in this Reissue Application. Claims 36-39 have been deleted. Claims 2-4,8-11,14,16-18,20,23, and 26-35 have been allowed. Claim 51 has been objected to and Claims 1,5-7,12,13,15,19,21,22,24,25,40-50,52,58 have been finally rejected by the Examiner.

IV. Status of Amendments

Since the final rejection of January 17,2002 an amendment was filed on March 5, 2002. In the Advisory Action mailed March 12, 2002 the Examiner indicated that the amendment would not be entered.

V. Summary of the Invention

The present invention generally relates to an infrared imaging system (Figure 1) having a focal plane array (col. 5, lines 1-3, Figure 2, item 10), The focal plane array includes an array of detector elements and a readout circuit (col. 5, lines 10-15 , Figures 3A-3C and 4) and includes non-uniformity correction circuitry on the focal plane array (col. 10, lines 2-16, Figure 2, item 10, and col. 11, lines 20-27). The individual detector elements (Figures 3A-3C, item 200, col. 11, lines 29-40) correspond to pixels of an infrared scene to be imaged. Offsets in detection signals from each pixel (Figures 3A-3C, item 200), arising from nonuniformities in the individual detector elements (Figures 3A-3C, item 200) in the array (Figure 2, item 10), are corrected by storing compensating offset correction values for each detector element; and using the stored offset values to control compensating correction circuitry as the respective

detector element signals are read out (col. 12, line 60 - col. 13, line 12).

VI. Issues

A. Are Claims 1,5,21,22,40,42, and 48 unpatentable under 35 U.S.C. 102(b) as being anticipated by Hegel, Jr., et al. (US 4752694A)?

B. Are Claims 6,7,12,13,15,19,24,25, 44-47, and 50 unpatentable under 35 U.S.C. 103(a) over Hegel, Jr. et al?

C. Do Claims 40-50 and Claims 52-58, rejected under 35 U.S.C. § 112, First Paragraph, contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention?

D. Do Claims 40-50 and Claims 52-58, rejected under 35 U.S.C. § 251, improperly recapture broadened claim subject matter surrendered in the application for the patent upon which the present reissue is based?

VII. Grouping of Claims

The claims do not stand or fall together. In accordance with 37 C.F.R. § 1.192(c)(7), the reasons why Appellants believe the claims to be separately patentable are contained in the Argument section below.

VIII. Arguments

The Examiner refused to enter the Amendment filed March 5, 2002. The Amendment filed March 5, 2002 merely corrected the dependency of Claim 51 from "1" to --40--. The Amendment was made to overcome the Examiner's objection under 37 C.F.R. 1.75 and simplify issues on appeal. The Examiner stated that the Amendment raised new issues. The Applicant's respectfully assert that the Examiner is incorrect. Changing the dependency of Claim 51 would not raise new issues. The Examiner also stated that the Amendment failed to comply with C.F.R. § 1.111(b). However, the Amendment was after a final rejection and 37 C.F.R. § 1.111(b) is not applicable to an amendment after a final rejection. The Board is requested to direct the Examiner to enter the Amendment filed March 5, 2002.

35 U.S.C sec. 102(b) Rejections

Claim 1 recites an infrared imaging system, having an infrared focal plane array. The focal plane array includes a plurality of infrared detector elements arranged in an array; a readout circuit electrically coupled to the plurality of detector elements and means for biasing the plurality of detector elements so as to provide separate detection signals corresponding to each detector element in the array; and means for separately correcting offsets in the detection signals provided from the plurality of elements in the detector array to compensate for nonuniformities in the detector elements. The means for correcting includes a correction circuit including a plurality of parallel connected circuit elements; and means for selectively electrically connecting said circuit elements into the detector readout circuit in response to stored offset correction values; and output means for providing the corrected detection signals

as an output of the focal plane array; means for storing a plurality of offset correction values corresponding to the plurality of detector elements; and means for providing the offset correction values to said means for correcting.

It should be appreciated that the present Claim 1's means for correcting offsets are distinctly different from Hegel's method of controlling current flow.

First, referring to the "Supplemental Examination Guidelines for Claims Subject to 35 U.S.C. 112, para. 6", the Applicant's respectfully point out that the guidelines state that "... a claim limitation will be interpreted to invoke 35 U.S.C. 112, para. 6 if it meets the following 3-prong analysis:

> (1) The claim limitations must use the phrase 'means for' or 'step for';
>
> (2) the 'means for' or 'step for' must be modified by functional language; and
>
> (3) the phrase 'means for' or 'step for' must not be modified by sufficient structure, or acts for achieving the specified function" [Footnote references omitted.]

It will be appreciated that the present Claim 1 uses the phrase 'means for' throughout the claim; the 'means for' are modified by functional language; and the 'means for' are not modified by sufficient structure for achieving the specified function. Indeed, the present Claim 1 'means for correcting' encompasses one structural element and four 'means for' elements. Therefore, the Applicants respectfully assert that the 'means for correcting' limitation of the present Claim 1 should be interpreted to invoke 35 U.S.C. § 112 para. 6.

Next, the same supplemental guidelines state that "the 'broadest reasonable interpretation' that an examiner may give means-plus-function language is that statutorily mandated in (35 U.S.C 112, para. 6)*** [T]he PTO may not disregard the structure disclosed in the specification corresponding to such language when rendering a patentability determination." *In re Donaldson Co.* 16 F.3d 1189, 1194-95, 29USPQ2d 1845,1850 (Fed. Cir 1994)(en banc). The guidelines also state that "The USPTO must apply 35 U.S.C. 112, para. 6 in appropriate cases, and give claims their broadest reasonable interpretation, in light of and consistent with the written description of the invention in the application." [Emphasis added.] [Footnote omitted.]

The same guidelines provide another 3-prong test for an examiner to make a prima facie case of 35 U.S.C. 112, para. 6 equivalence. This 3-prong test states that if the examiner finds that a prior art element (1) performs the function specified in the claim, (2) is not excluded by any explicit definition provided in the specification for an equivalent, and (3) is an equivalent of the means-(or step) plus-function limitation, the examiner should provide a rational as to why the prior art element is equivalent.

Here, the Applicants respectfully direct the Board's attention to column 3, lines 61-63 of the present reissue application, which states that the "... circuit elements may comprise a plurality of capacitors or constant current sources". This is an explicit definition provided in the specification excluding equivalents other than capacitors or constant current sources with regards to offset correction means. Therefore, in light of this explicit statement and the referenced guidelines, the Applicants respectfully assert that the Examiner has not made a prima facie case of equivalence with regard to Hegel.

The lack of Hegel's equivalence is further demonstrated by considering the "means for" language of the present Claim 1 and any one of the embodiments shown in Figures 3B-3C,4, 10, or 11, of the present application. Figure 3B, for example, shows a correcting voltage that is applied to the output V_{out} at point 222 where it either adds to, or subtracts from, the voltage held by sample and hold capacitor 212. Similarly, Figures 10-12 show current sources (I_o-I_n) added directly to the detector bias current.

Giving Claim 1 of the present application its broadest reasonable interpretation, in light of and consistent with the written description of the invention in the application, nowhere in Hegel's path is a correcting offset applied.

Moreover, it is clear from Hegel's description that since the FETs (44-46) are biased either full-on or full-off, there is effectively an electrical short circuit between the diodes D and point B (col. 2, lines 22-53) with no disclosure or suggestion of any offset corrections as encompassed by the language of the present means for language of the present Claim 1.

The Examiner, in paragraph 19 of the Final Office Action (dtd 1/17/02) states that Hegel's figure 5 discloses an offset correction circuit. However, it will be appreciated that the offset correction circuit shown in Hegel's figure 5 is a single offset correction circuit that does not directly add or subtract offsets, but rather is part of an indirect system which adds a voltage to fixed power supply V_F which in turn controls the amount of current flow through preamp transistor 51 and load resistor R_L. It will be understood that the detector output voltage to Hegel's readout circuit will be a function of the size of the load resistor R_L and the amount of current through that load resistor. It will be readily appreciated that this is not

the same as directly adding an offset voltage to a detector voltage or adjusting bias current through a detector as is encompassed by the present Claim 1's means plus function language and shown in Figures 3B-3C,4,10, or 11, of the present application.

Likewise, Hegel's figure 4 also controls current flow through preamp transistor 51 by adding a voltage to fixed power supply V_F. Here Hegel allows the selection of a voltage through voltage divider network 82 and another fixed power supply V_E to be added to fixed power supply V_F with the same result of controlling current flow through preamp transistor 51 and load resistor R_L. It will again be readily appreciated that this is not the same as adding an offset voltage to a detector voltage held by a capacitor or adjusting bias current through the detector as is encompassed by the present Claim 1's means plus function language and shown in Figures 3B-3C,4,10, or 11, of the present application.

It will also be readily apparent to one moderately skilled in the art that the fixed power supplies V_F and V_E and resistors R_1-R_{15} do not disclose or suggest the offset correcting capacitors or current sources shown in Figures 3B-3C,4,10, or 11, of the present application. It will be appreciated that current sources as represented in the present application (Figures 10-12) have different characteristics and operating parameters than the simple $V_{F,E}/R$ network shown in Hegel's figure 4.

As shown above, the means-for language of the present Claim 1, interpreted in light of and consistent with the written description of the invention in the application, recites separately correcting offsets by directly adding or subtracting a voltage or current directly to a detector voltage or current, respectfully. This element is not seen or suggested by Hegel.

Next, the Examiner states that Hegel's memory (fig. 1, item 70) stores offset correction values. The Applicants respectfully disagree. Hegel's memory holds biasing values for controlling how much current is allowed to flow through a particular Hegel detector. This is made clear by referring to Hegel's figure 1, where it can be seen that Hegel's biasing values are applied to the gates of FETs 14-16. It will be readily appreciated by those skilled in the art that gates of FET devices do not provide an electrical path to either the source or drain of the FET. The gate controls the amount of current flow through the FET by changing the "FET ON-resistance" (col. 2, line 65 - col. 3, line 10). It will be further readily appreciated that since a FET gate does not have a direct electrical path to either the source or drain, a voltage appearing on the gate may not be used to directly offset a drain or source voltage.

Therefore, since all the elements of Claim 1 are not anticipated in view of Hegel, Claim 1 is patentable and should be allowed.

Claim 5 recites an infrared imaging system as set out in Claim 1, wherein the means for selectively connecting comprises a plurality of switches, equal in number to the plurality of parallel connected circuit elements and connected in series therewith. As pointed out above and repeated here, Hegel does not apply offsets but rather controls current flow through FETs 14-16. It follows therefore, that since Hegel does not disclose or suggest applying offsets, that Hegel does not, disclose or suggest a plurality of switches series connected to a respective plurality of parallel circuit elements. This is intuitively obvious from the above discussion where it is shown that Hegel does not disclose or suggest applying offsets (voltage or current).

Claim 5 recites an infrared imaging system as set out in Claim 1, wherein the means for selectively connecting comprises a plurality of switches, equal in number to the plurality of parallel connected circuit elements and connected in series therewith. This is not disclosed or suggested in Hegel. Therefore, Claim 5 is not anticipated in view of Hegel and is patentable and should be allowed.

Claim 21 of the present application recites timing means for providing focal plane timing signals to the readout circuit. The Examiner states that Hegel anticipates this claim by providing "clock input" to the readout circuit. However, the only thing that Hegel says in this regard is that the sequencer provides the signals necessary to synchronize the operation of memory, switch, and the readout circuit. As pointed out above and repeated here, Hegel's sequencer (Figure 5, item 62) synchronizes which FET 44-46 is turned on to allow current flow through transistor 51" and load resistor R_L. It will be appreciated that this is not the same as providing a timing signal to a readout circuit to control readout and offset correction applied to a node common with a detector (Figure 3B of the present application).

Claim 21 of the present application recites timing means for providing focal plane timing signals to the readout circuit. As described above, Hegel does not disclose or suggest this element. Therefore, Claim 21 is not anticipated by Hegel and is patentable and should be allowed.

Claim 22 of the present application recites the features that the readout circuit comprises offset correction logic means for controlling the means for correcting in response to the timing signals presented to the readout circuit. As pointed out above, and repeated here, Hegel does not provide timing signals to the readout circuit or suggest offset correction logic means for

controlling the means for correcting. Therefore, Claim 22 is patentable and should be allowed.

Claim 40 of the present application recites an infrared imaging system. The claimed system comprises an infrared focal plane array, which in turn, comprises a plurality of infrared detector elements arranged in an array. Claim 40 also recites the claim element of a correction circuit including a plurality of circuit elements for separately correcting offsets in the detection signals to compensate for nonuniformities in the detector elements. As explained above, it should be appreciated that the present Claim 40's correcting offsets (e.g., voltages or currents) are distinctly different from Hegel's method of controlling current flow. This is made clear by first considering, for example, the "means for" language of the present Claim 40 and any one of the embodiments shown in Figures 3B-3C,4, 10, or 11, of the present application. Figure 3B, for example shows a correcting voltage that is applied to the output V_{out} at point 222 where it either adds to, or subtracts from, the voltage held by sample and hold capacitor 212. Similarly, Figures 10-12 show current sources (I_o-I_n) added directly to the detector current.

Again, consider Hegel. First, it is immediately apparent that nowhere does Hegel disclose or suggest a sample and hold capacitor in the output path of a detector diode (Hegel figure 1, items 11/D). Second, nowhere does Hegel disclose or suggest applying correcting offsets (i.e., adding to or subtracting from) to the detectors, Hegel figure 1, items 11). Indeed, examining Hegel's figure 1 shows the output of the detectors 11 through diodes D and then through a FET to point B and then to readout circuit 51. Nowhere in this path is a correcting offset applied.

Moreover, it is clear from Hegel's description that since the FETs (44-46) are biased either full-on or full-off, there is effectively an electrical short between the diodes D and point B (col. 2, lines 22-53) and no disclosure or suggestion of any offset corrections.

Next, the Examiner states that Hegel's memory (fig. 1, item 70) stores offset correction values. The Applicants respectfully disagree. Hegel's memory holds biasing values for controlling how much current is allowed to flow through a particular Hegel detector. This is made clear by referring to Hegel's figure 1, where it can be seen that Hegel's biasing values are applied to the gates of FETs 14-16. It will be readily appreciated by those skilled in the art that gates of FET devices do not provide an electrical path to either the source or drain of the FET, but rather, the gate controls the amount of current flow through the FET by changing the "FET ON-resistance" (col. 2, line 65 - col. 3, line 10). It will be further readily appreciated that since a FET gate does not have a direct electrical path to either the source or drain, a voltage appearing on the gate may not be used to directly offset a drain or source voltage. Nor, as pointed out, does Hegel, disclose or suggest applying correcting offsets. The Examiner, in paragraph 19 of the Final Office Action (dtd 1/17/02) states that Hegel's figure 5 discloses an offset correction circuit. However, it will be appreciated that the offset correction circuit shown in Hegel's figure 5 is a single offset correction circuit that does not add or subtract offsets but rather controls current flow through transistor 51" and load resistor R_L. This is not the same as directly adding or subtracting an offset correction as in the present invention. Furthermore, nowhere does Hegel disclose or suggest separately correcting offsets by directly adding or subtracting a voltage or

current as shown in the present application figures. Therefore, Claim 40 is patentable and should be allowed.

Claim 40 recites the claim element of a correction circuit including a plurality of parallel connected circuit elements for separately correcting offsets in the detection signals to compensate for nonuniformities in the detector elements, as described above. This is not disclosed or suggested in Hegel. Therefore, since Claim 40 is not anticipated in view of Hegel, Claim 40 is patentable and should be allowed.

Claim 42 of the present invention recites an infrared imaging system as set out in claim 40. Claim 42 further recites means for selectively connecting a plurality of switches, equal in number to the plurality of circuit elements and connected in series therewith. In rejecting this claim the Examiner points to Hegel's figure 1 switches A,B,C and FETs 14,15,16 as anticipating Claim 42. However, as pointed out above, switches A,B, & C merely route bias voltages to the FET gates and do not selectively apply an offset. Next, it will be appreciated that the Hegel switches A,B, & C are not in series with FETs 14,15, & 16, as recited in the present claim.

Claim 42 recites an infrared imaging system as set out in Claim 40, wherein the means for selectively connecting comprises a plurality of switches, equal in number to the plurality of parallel connected circuit elements and connected in series therewith. This is not disclosed or suggested in Hegel. Therefore, Claim 42 is not anticipated in view of Hegel and is patentable and should be allowed.

35 U.S.C. sec. 103(a) Rejections

Claim 6 recites an infrared imaging system as set out in claim 1, wherein the offset correction values (i.e., the switch selecting values) are binary values and wherein the means for storing the offset correction values comprises a digital memory. As pointed out above, Hegel does not apply corrective offsets and therefore does not disclose or suggest storing binary offset correction values. Indeed, this is made clear by considering Hegel figures 1,4, or 5, and observing that Hegel switches A,B, and C, merely route transistor biasing voltages to Hegel FETS 14-16. Therefore, since the Claim 6 feature of storing binary offset correction values for applying corrective offsets is not disclosed or suggested in Hegel, Claim 6 is not obvious in view of Hegel. Thus, Claims 6-7 are patentable and should be allowed.

Claim 12 of the present application recites the features of forming the detector array and the readout circuit on a single monolithic integrated circuit chip. The Examiner rejected this claim with the statement that it would have been obvious to one of ordinary skill to form on a single monolithic IC the system illustrated by Hegel. With regards to Hegel's system (not modified with the present invention), that may be true. However, whether or not Hegel's system could be formed on a monolithic IC has no bearing on whether or not the present invention could be formed on a monolithic IC. Therefore, since the Claim 12 feature of forming the detector array and the readout circuit of the present invention on a single monolithic integrated circuit chip is not disclosed or suggested in Hegel, Claim 12 is not obvious in view of Hegel. Thus, Claim 12 is patentable and should be allowed.

Claim 13 of the present application recites the feature that the detector elements of Claim 1 comprise micro-bolometer detector elements. In rejecting this Claim the Examiner points to Hegel and states that Hegel is a bolometer and that the choice of size is a choice within the ordinary skill in the art. However, Hegel does not disclose or suggest applying offsets to the Hegel bolometers and, by extension, Hegel does not disclose applying offsets to micro-bolometers. Therefore, Claim 13 is not obvious in view of Hegel and is patentable and should be allowed.

Claim 15 of the present application recites the feature of a fixed voltage source coupled to the miniaturized micro-bolometers recited in Claim 13. As noted, the micro-bolometers of the present application are well beyond the ordinary skill represented in Hegel and that Hegel does not disclose or suggest applying offsets to such micro-bolometers. Therefore, Claim 15 is not obvious in view of Hegel and is patentable and should be allowed.

Claim 19 of the present application recites the feature of the output means comprising one or more buffers. In rejecting this claim, the Examiner states that it would have been obvious to one of ordinary skill to include buffers in view of the circuit protection that would have been provided. However, the Applicants respectfully point out that buffers are not just for circuit protection and therefore the inclusion of such is not obvious. First, there is no suggestion in Hegel to add such buffers nor is it obvious to one skilled in the art to simply add buffers to Hegel. Indeed, adding buffers could cause synchronization problems, increase current drain, increase operating temperature, and so on. Clearly, adding buffers is not an obvious or trivial

step.

Therefore, since the Claim 19 feature of the output means comprising one or more buffers is not disclosed or suggested in Hegel, Claim 19 is not obvious in view of Hegel. Thus, Claim 19 is patentable and should be allowed.

Claim 24 of the present application recites an infrared imaging system comprising means for analog-to-digitally converting (ADC) the corrected detection signals, and providing corresponding image data for each detector element. Hegel, on the other hand, merely provides output means to a "preamp and readout circuit", (Hegel Figure 1). There is no suggestion anywhere in Hegel that Hegel's readout circuit contain an ADC. Indeed, the Hegel preamp shown in Hegel's figure 1 suggests that the Hegel readout is in the analog domain and not the digital domain. Therefore, since Hegel does not suggest or disclose the Claim 12 feature of analog-to-digitally converting (ADC) the corrected detection signals, and providing corresponding digital image data for each detector element, Claim 24 is patentable and should be allowed.

Claim 25 of the present application recites a memory for storing image data corresponding to all the detector elements of the array. Again, Hegel merely shows a preamp and readout circuit. Nowhere does Hegel disclose or suggest that this readout circuit stores digital image data. It will be appreciated that the Hegel readout circuit is not the same, nor can it be reasonably construed to be the same, as a memory device. Therefore, since Hegel does not disclose or suggest the Claim 25 feature of a memory for storing image data corresponding to all the detector elements, Claim 25 is not obvious in view of Hegel. Thus, Claim

25 is patentable and should be allowed.

Claim 44 of the present application recites an infrared imaging system comprising means for analog-to-digitally converting (ADC) the corrected detection signals, and providing corresponding image data for each detector element. As pointed out above, and repeated here, Hegel merely provides output means to a "preamp and readout circuit", (Hegel Figure 1). There is no suggestion anywhere in Hegel that Hegel's readout circuit contain an ADC. Indeed, the Hegel preamp shown in Hegel's figure 1 suggests that the Hegel readout is in the analog domain and not the digital domain. Therefore, since Hegel does not suggest or disclose the Claim 44 features of analog-to-digitally converting (ADC) the corrected detection signals, and providing corresponding digital image data for each detector element, Claim 44 is not obvious in view of Hegel. Thus, Claim 44 is patentable and should be allowed.

Claim 45 of the present application recites the feature that the detector elements of Claim 40 comprise micro-bolometer detector elements. In rejecting this Claim the Examiner again points to Hegel and states that Hegel is a bolometer and that the choice of size is a choice within the ordinary skill in the art. However, as pointed out above, Hegel does not disclose or suggest applying offsets to the Hegel bolometers and, by extension, Hegel does not disclose applying offsets to micro-bolometers. Therefore, since Hegel does not disclose or suggest the Claim 45 feature of applying offsets to micro-bolometers, Claim 45 is not obvious in view of Hegel. Thus, Claim 45 is patentable and should be allowed.

Claim 46 recites an infrared imaging system as set out in claim 1, wherein the offset correction values (i.e., the switch selecting values) are binary values and wherein the means for storing the offset correction values comprises a digital memory. As pointed out above Hegel does not apply corrective offsets and therefore does not disclose or suggest storing binary offset correction values. Indeed, this is made clear by considering Hegel figures 1,4, or 5, and observing that Hegel switches A,B, and C, merely route transistor biasing voltages to Hegel FETS 14-16. Therefore, since Hegel does not disclose or suggest the Claim 46 feature, where offset correction values are binary values and wherein the means for storing the offset correction values comprises a digital memory, Claim 46 is not obvious in view of Hegel. Thus, Claim 46 is patentable and should be allowed.

Claim 47 of the present application recites the features of forming the detector array and the readout circuit on a single monolithic integrated circuit chip. The Examiner rejected this claim with the statement that it would have been obvious to one of ordinary skill to form on a single monolithic IC the system illustrated by Hegel. With regards to Hegel's system (not modified to include the present invention), that may be true. However, whether or not Hegel's system could be formed on a monolithic IC has no bearing on whether or not the present invention could be formed on a monolithic IC. Therefore, since Hegel does not disclose or suggest the Claim 47 features of forming the detector array and the readout circuit on a single monolithic integrated circuit chip, Claim 47 is not obvious in view of Hegel. Thus, Claim 47 is patentable and should be allowed.

Claim 50 of the present application recites the feature of the output means comprising one or more buffers. In rejecting this claim, the Examiner again states that it would have been obvious to one of ordinary skill to include buffers in view of the circuit protection that would have been provided. However, the Applicants respectfully point out that buffers are not just for circuit protection and therefore the inclusion of such is not obvious. First, there is no suggestion in Hegel to add such buffers nor is it obvious to one skilled in the art to simply add buffers to Hegel. Indeed, adding buffers could cause synchronization problems, increase current drain, increase operating temperature, and so on. Clearly, adding buffers is not an obvious or trivial step. Therefore, since Hegel does not disclose or suggest the Claim 50 feature of the output means comprising one or more buffers, Claim 50 is not obvious in view of Hegel. Thus, Claim 50 is patentable and should be allowed.

35 U.S.C. § 251 Rejections

The Examiner has rejected claims 40-50 and 52-58 as being an improper recapture of broadened claimed subject matter surrendered during prosecution of the original application for the patent upon which the present reissue is based. Specifically, the Examiner points to amended reissue claims 40,41,42,43,52, and 58, as deleting the limitation "parallel connected" and states that this renders the reissue claims as broader in scope than the issued patent claims. The Examiner points to the language used by the first Examiner in allowing the original application ("...the means for correcting specified by independent claim 2,24,33, or 37.") and MPEP sec. 1412.02, and states that the applicants previously surrendered the now broader aspect of the reissue claims during prosecution of the original application since the

Applicants did not present on the record a counter statement or comment as to the Examiner's reasons for allowance.

In MPEP § 1412.02, under the section entitled "Criteria For Determining That Subject Matter Has Been Surrendered:", three examples are listed. Example "C" is the closest to the facts of the present case. Example "C" states:

> (C) The limitation A omitted in the reissue claims was present in the claims of the original application. The examiner's reasons for allowance in the original application stated that it was that limitation A which distinguished over a potential combination of references X and Y. Applicant did not present on the record a counter statement or comment as to the examiner's reasons for allowance, and permitted the claims to issue. The omitted limitation is thus established as relating to subject matter previously surrendered.

In the present case, the claim limitation "parallel connected" was in claims 1,2,5,9, and 26, as originally filed on September 12, 1996. The limitation "parallel connected" was not argued by Applicants' attorney during prosecution of the application. In the Notice of Allowability issued December 9, 1997 the first Examiner stated:

> "The following is an examiner's statement of reasons for allowance: the prior art of record fails to teach or fairly suggest an infrared imaging system or focal plane array having in combination with the other required elements, the means for correcting specified by independent claim 2,24,33, or 37. Claims not addressed are allowable by virtue of their dependency."

MPEP sec. 1412.02, example C, requires "limitation A" to be stated in the Examiner's reason for allowance in order to prevent "limitation A" from being omitted in the reissue claim. In the

present case the limitation being omitted (i.e., "limitation A") is "parallel connected". Yet, the first Examiner's reason for allowance did not state that the reason for allowance was because the claims contained the limitation "parallel connected". The first Examiner's reason for allowance was because "...the prior art of record fails to teach or fairly suggest an infrared imaging system or focal plane array having in combination with the other required elements, the means for correcting specified by independent claims 2,24,33, or 37." The first Examiner's reason for allowance is not specific to the limitation: "parallel connected".

Example A of the same MPEP section can serve as an analogous model, instructive in teaching specific limitation language. In Example A the situation is reversed; i.e., the example is directed towards an applicant arguing the limitation. Using this example, the MPEP points out that the argument must be specific to the limitation and not a general statement. MPEP page 1400-0, col. 1, lines 7-17, states:

> "The argument that the claim limitation defined over the rejection must have been specific as to the limitation; rather than a general statement regarding the claims as a whole. In other words, a general 'boiler plate' sentence will not be sufficient to establish recapture." [Emphasis added.]

Keeping this MPEP specific limitation rule in mind (albeit by an applicant), it appears that the present Examiner has mischaracterized the first Examiner's reasons for allowance. The first Examiner states that the prior art did not teach or suggest a system "... an infrared imaging system or focal plane array

having in combination with other required elements, the means for correcting...". However, it is clear that (1) this was a general statement by the first Examiner and (2) that the first Examiner did not specifically state the limitation of "parallel connected" in the reason for allowance. Indeed, nowhere in the Notice of Allowability does the word "parallel" appear. The first Examiner's reason for allowance was the "combination" of a means for correcting with the other claim elements. Thus, the first Examiner's statement can only be regarded as a general statement; not a specific statement regarding "parallel connection".

Therefore, reissue claims 40,41,42,43,52, and 58 do not improperly recapture broadened claimed subject matter. Nor do reissue claims 40,41,42,43,52, and 58 contain subject matter surrendered during prosecution of the original application for the patent upon which the present reissue is based. Therefore reissue claims 40,41,42,43,52, and 58, are patentable and should be allowed.

Similarly, the present Examiner also states the reissue Claim 53 deletes a limitation, i.e., "capacitors" thus rendering the reissue claim broader than the patent claim. The Examiner also states that the Applicant surrendered this broader aspect during the prosecution of the original application.

The Applicants respectfully point out that the word "capacitors" does not appear in the first Examiner's reason for allowance and that the first Examiner's reason for allowance was a general statement; that this general statement is not specific as contemplated by the MPEP sec. 1412.02. Therefore, the Applicants respectfully submit that the broadened aspect of the present reissue Claim 53 is not previously surrendered subject matter and

that the present reissue Claims 53-57 are patentable and should be allowed.

35 U.S.C. sec. 112, first paragraph

Claims 40-50 and 52-58 were rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter that was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors had possession of the claimed invention.

The Examiner states that the specification does not describe a system in which the circuit elements are not parallel connected. Specifically, the Examiner points to figures 3B and 3C where there is shown a plurality of circuit elements, i.e., capacitors and switches, parallel connected, and indicates that the specification does not support any other interpretation other than a parallel connection.

First, it should be recognized that capacitors C_0, C_1, $C_2 \ldots C_N$, and their associated switches S_0, S_1, $S_2 \ldots S_N$, represent the offset correction circuit 220 shown in figure 3B, which is only a preferred implementation and not a limitation to only plural, parallel connected capacitors and switches. This is made clear by recognizing that the series representations (i.e., C_0, C_1, $C_2 \ldots C_N$, and S_0, S_1, $S_2 \ldots S_N$) are well known in the art and that the identifying variable N can range from integer value 0 to any positive integer value. Moreover, it is clear that for $N = 0$, there is only one capacitor-and-switch branch which, by definition, cannot be "parallel connected". Likewise, if $N > 0$ but only one switch in figure 3B, S_0 for example, is closed, and

all the other switches S_1-S_N are open, then only one branch is connected. Again, this would be a situation in which the branch cannot be in parallel with the other branches. In this situation (only S_0 closed) there is only one functioning capacitor, C_0; capacitors C1-CN are not functionally operational; and the system is only using the capacitance associated with the single capacitor C_0.

The Examiner also states, with regard to current sources, that the specification does not describe a system in which the circuit elements are not parallel connected. The Applicants respectfully point out that the current sources are similarly represented as I_0...I_N and that even one moderately skilled in the art recognizes that N can be any value between 0 and any positive integer; and that for a N=0 situation there is only one current branch which by definition cannot be parallel connected. Thus, again, to one even moderately skilled in the art, the specification more than reasonably conveys that the Applicants had possession of the claimed invention.

It will also be appreciated that in paragraph 19 of the Examiner's Final Office Action (January 17, 2002) the Examiner, in support of the Examiner's claim that only a parallel connection is shown, has mischaracterized the Applicants' argument and states that the Applicants' argument is "bizarre" and further states that the claims 40,52,53, and 58 "demand a plurality of circuit elements" and thus incorrectly reasons that only a parallel connected implementation is possible. However, "a correction circuit including a plurality of circuit elements (Claim 40) as shown in Figures 3B,3C,10 and 11 of the present invention may consist of only one switch (S_0) and only one capacitor (C_0). In other words, switch S_0 and capacitor C_0 may be

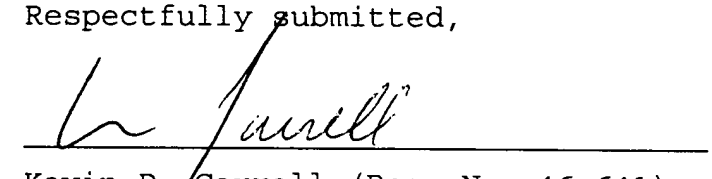
the plurality of circuit elements. It will be further appreciated that for N=0, only switch S_0 and capacitor C_0 are present and are series connected.

Therefore, the Applicants respectfully submit that the now broader reissue claims without the limitation "parallel connected" is not impermissible recapture of surrendered subject matter and that Claims 40-50, and 52-58, are not in violation of 35 U.S.C. § 112, 1st paragraph and, therefore, are patentable and should be allowed.

IX. Conclusion

In view of the arguments presented above, it is respectfully requested that the Examiner's rejections of Claims 1,5,7,12,13,15,19,21,22,24,25,40-50,52,58 be reversed.

Respectfully submitted,



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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231.

June 10, 2002.
Date

Victoria Porter
Name of Person Making Deposit

Appendix A

Rejected Claims

1. An infrared imaging system, comprising:

an infrared focal plane array comprising:

a plurality of infrared detector elements arranged in an array;

a readout circuit electrically coupled to the plurality of detector elements and comprising means for biasing the plurality of detector elements so as to provide separate detection signals corresponding to each detector element in the array, in response to incident infrared radiation and means for separately correcting offsets in the detection signals provided from the plurality of elements in the detector array to compensate for nonuniformities in the detector elements, wherein said means for correcting comprises:

a correction circuit including a plurality of parallel connected circuit elements; and

means for selectively electrically connecting said circuit elements into the detector readout circuit in response to stored offset correction values; and

output means for providing the corrected detection signals as an output of the focal plane array;

means for storing a plurality of offset correction values corresponding to the plurality of detector elements; and

means for providing the offset correction values to said means for correcting.

5. An infrared imaging system as set out in claim 1, wherein said means for selectively connecting comprises a plurality of switches, equal in number to said plurality of parallel connected circuit elements and connected in series therewith.

6. An infrared imaging system as set out in claim 1, wherein said offset correction values are binary values and wherein said means for storing comprises a digital memory.

7. An infrared imaging system as set out in claim 6, wherein said digital memory stores a separate binary offset correction value for each detector element in the array.

12. An infrared imaging system as set out in claim 1, wherein said array of detector elements and said readout circuit are formed as a single monolithic integrated circuit chip.

13. An infrared imaging system as set out in claim 1, wherein said plurality of detector elements comprise microbolometer detector elements.

15. An infrared imaging system as set out in claim 13, wherein said means for biasing comprises a fixed voltage source coupled to said microbolometer detector elements.

19. An infrared imaging system as set out in claim 1, wherein said output means comprises one or more output buffers.

21. An infrared imaging system as set out in claim 1, further comprising timing means for providing focal plane timing signals to said readout circuit.

22. An infrared imaging system as set out in claim 21, wherein said readout circuit further comprises offset correction logic means for controlling the means for correcting in response to said timing signals provided from the timing means.

24. An infrared imaging system as set out in claim 1, further comprising means, coupled to said output means, for analog to digital converting the corrected detection signals and providing corresponding image data for each detector element.

25. An infrared imaging system as set out in claim 24, further comprising a memory for temporarily storing image data corresponding to all the detector elements of the array.

40. An infrared imaging system, comprising:

an infrared focal plane array comprising:

a plurality of infrared detector elements arranged in an array;

a readout circuit electrically coupled to the plurality of detector elements and comprising means for biasing the plurality of detector elements so as to provide separate detection signals corresponding to each detector element in the array, in response to incident infrared radiation and means for separately correcting offsets in the detection signals provided from the plurality of elements

in the detector array to compensate for nonuniformities in the detector elements, wherein said means for correcting comprises:

a correction circuit including a plurality of circuit elements; and

means for selectively electrically connecting said circuit elements into the detector readout circuit in response to stored offset correction values; and

output means for providing the corrected detection signals as an output of the focal plane array;

means for storing a plurality of offset correction values corresponding to the plurality of detector elements; and

means for providing the offset correction values to said means for correcting.

41. An infrared imaging system as set out in claim 40, wherein said plurality of circuit elements comprise a plurality of capacitors.

42. An infrared imaging system as set out in claim 40, wherein said means for selectively connecting comprises a plurality of switches, equal in number to said plurality of circuit elements and connected in series therewith.

43. An infrared imaging system as set out in claim 40, wherein said plurality of circuit elements comprise a plurality of constant current sources.

44. An infrared imaging system as set out in claim 40, further comprising means, coupled to said output means, for analog to digital converting the corrected detection signals and providing corresponding image data for each detector element.

45 An infrared imaging system as set out in claim 40, wherein said plurality of detector elements comprise microbolometer detector elements.

46. An infrared imaging system as set out in claim 40, wherein said offset correction values are binary values and wherein said means for storing comprises a digital memory.

47. An infrared imaging system as set out in claim 40, wherein said array of detector elements and said readout circuit are formed as a single monolithic integrated circuit chip.

48. An infrared imaging system as set out in claim 40, further comprising timing means for providing focal plane timing signals to said readout circuit.

49 An infrared imaging system as set out in claim 40, wherein said plurality of detector elements are arranged in a plurality of rows and columns and wherein said means for correcting comprises a separate offset correction circuit for each column and wherein said means for providing said offset correction

values provides said offset correction values in a time multiplexed manner to said means for correcting.

50. An infrared imaging system as set out in claim 40, wherein said output means comprises one or more output buffers.

51. An infrared imaging system as set out in claim 1, wherein said focal plane array further comprises a differential amplifier with first and second inputs wherein the first input is electrically connected to the readout circuit so as to receive the detection signals and wherein the second input is connected to an adjustable reference voltage.

52. An infrared imaging system, comprising:

an infrared focal plane array comprising:

a plurality of infrared detector elements arranged in an array;

a readout circuit electrically coupled to the plurality of detector elements and comprising a plurality of readout cells equal in number to the plurality of detector elements, means for biasing the plurality of detector elements so as to provide separate detection signals corresponding to each detector element in the array, in response to incident infrared radiation and means for separately correcting offsets in the detection signals provided from the plurality of

elements in the detector array to compensate for nonuniformities in the detector elements, wherein said means for correcting comprises an offset correction circuit in each readout cell of the readout circuit and wherein each offset correction circuit comprises a plurality of circuit elements and means for selectively electrically connecting said circuit elements into the readout cell in response to a stored offset correction value corresponding to said readout cell; and

output means for providing the corrected detection signals as an output of the focal plane array;

means for storing a plurality of offset correction values corresponding to the plurality of detector elements; and

means for providing the offset correction values to said means for correcting.

53. An infrared focal plane array, comprising:

a plurality of detector elements configured in a two dimensional array; and

a readout circuit electrically coupled to said plurality of detector elements and structurally integrated therewith, said readout circuit comprising:

a sample and hold capacitor;

means for biasing the detector elements so as to provide an analog detection signal from each detector element corresponding to the infrared radiation incident thereon, wherein the analog detection signal is a voltage signal provided at a sample node coupled to the sample and hold capacitor; and

means for correcting the analog detection signal from each detector element by a discrete offset correction and providing a corrected analog detection signal, wherein the discrete offset correction varies from detector element to detector element and comprises an offset correction voltage added to, or subtracted from, the analog detection signal, wherein said means for correcting subtracts or adds a variable amount of charge from said sample and hold capacitor to provide a corrected voltage signal at said sample node, and wherein said means for correcting comprises a plurality of circuit elements connected between said sample node and a reference voltage and a corresponding plurality of switches coupled in series with each respective circuit element and said reference voltage, wherein said plurality of switches selectively provide a desired amount of discrete offset correction for each detector element.

54. An infrared focal plane array as set out in claim 53, wherein said readout circuit further comprises means for controlling said means for correcting so as to selectively open and close said plurality of switches in a time multiplexed manner during readout of a plurality of separate detector elements.

55. An infrared focal plane array as set out in claim 53, wherein said detector elements comprise microbolometer detector elements.

56. An infrared focal plane array as set out in claim 53, wherein said readout circuit further comprises a differential amplifier having first and second inputs, the first input thereof coupled to said sample node and said second input thereof coupled to a adjustable voltage source.

57. An infrared focal plane array as set out in claim 53 wherein said plurality of detector elements and said readout circuit are formed as a single monolithic integrated circuit wherein said readout circuit acts as a substrate for said detector elements.

58. An infrared focal plane array, comprising:

a plurality of detector elements configured in a two dimensional array; and

a readout circuit electrically coupled to said plurality of detector elements and structurally integrated therewith, said readout circuit comprising:

a sample and hold capacitor;

means for biasing the detector elements so as to provide an analog detection signal from each detector element corresponding to the infrared radiation incident thereon, wherein the analog detection signal is a voltage signal

provided at a sample node coupled to the sample and hold capacitor; and

means for correcting the analog detection signal from each detector element by a discrete offset correction and providing a corrected analog detection signal, wherein the discrete offset correction varies from detector element to detector element and comprises an offset correction voltage added to, or subtracted from, the voltage signal, wherein said means for correcting subtracts or adds a variable amount of charge from said sample and hold capacitor to provide a corrected voltage signal at said sample node, and wherein said means for correcting comprises a plurality of constant current sources connected between said sample node and a reference voltage and a plurality of switches corresponding to said plurality of constant current sources and respectively coupled in series therewith.